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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,016	12/02/2003	Serguei M. Belousov	2230.0020000/MBR/GSB	3183
54089 7590 11/16/2007 BARDMESSER LAW GROUP, P.C. 910 17TH STREET, N.W. SUITE 800 WASHINGTON, DC 20006			EXAMINER NGUYEN, PHILLIP H	
			ART UNIT 2191	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/725,016

Applicant(s)

BELOUSSOV ET AL.

Examiner

Phillip H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-73 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 13-30, 35-43, 48-56 and 61-73 is/are rejected.
- 7) ☒ Claim(s) 9-12, 31-34, 44-47, 57, 59 and 60 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. This action is in response to the amendment filed 9/3/2007.
2. Claims 1-73 are pending and have been considered below.

#### ***Response to Amendment***

3. The object to the abstract is withdrawn in view of Applicants' amendment to reduce the number of words to fewer than 150.
4. The objection to claim 59 is withdrawn in view of Applicants' amendment to correct the identified discrepancy.
5. Claims 67 and 68 have been amended to recite "a computer usable recording medium" to overcome the 101 non-statutory rejection. However, a computer usable recording medium" still covers signals (see specification paragraph [0082]). Therefore, examiner maintains his rejection to claims 67-68.

#### ***Response to Arguments***

6. Applicant's arguments filed 9/3/2007 have been fully considered but they are not deemed persuasive.

Applicant asserts on pages 18-20 of the amendment that Deusterwald fails to teach or deal with individual instructions. More importantly, Deusterwald makes no distinction between instructions that can be used as countable "mark" instructions and any other instruction. Thus, even if a function contains only one instruction to be a countable instruction, it can be any

instruction. In sum, Duesterwald lacks the concept of mark instructions as that term is defined in the specification and recited in the claims.

Examiner respectfully disagrees with the allegation as argued. Firstly, Duesterwald teaches “*system and method for dynamically patching code*” (see at least the Title). Secondly, the claimed limitations do not limit to individual instructions. For example, claim 1 recites “*identifying original instructions...copying the original instructions...replacing original instructions...*” In other words, claim 1 deals with fragments of instructions which are groups of instructions. Thirdly, the claimed limitations also do not limit that only mark instructions are countable. Thus, even if Duesterwald makes no distinction between instructions that are used as countable “mark” instructions and any other instruction. Duesterwald still teaches the claimed limitation, which are mark instructions are countable. More importantly, the claimed limitation does not teach counting the mark instructions. The claimed limitation discloses that the mark instructions are countable (functional language). In other words, the mark instructions can be counted using any technique. Persons of ordinary skill in the art can recognize counting instructions are well known to the art whether using tag, mark, counter, etc.

Applicant asserts on page 21 of the amendment that Duesterwald fails to teach copy original instructions to another location in memory to generate pseudooriginal instructions.

Examiner respectfully disagrees with the allegation as argued. Duesterwald teaches “*the application’s binary image can be copied to a temporary location*” (see at least paragraph [0024]). Furthermore, Duesterwald teaches “*an instruction fetch controller 128 can then be used to extract (i.e., fetch) copies of fragments (e.g., traces) of the application binary code, pass them to the DELI core 106 for caching, and direct the core 106 to execute the appropriate*

*cached copies out of its code cache 124*” (also see at least [0026]). Therefore, Duesterwald does teach copy original instructions to another storage location.

Applicant asserts on pages 23-24 of the amendment that Duesterwald fails to teach masking interrupts rather Duesterwald teaches replacing certain system calls the code with other system calls that are compatible with the hardware for which Duesterwald is patching the code.

Examiner respectfully disagrees with the allegation as argued. Duesterwald teaches “...*Implementation of the policies controls the manner in which the DELI 100 reacts to specific system and/or hardware events (e.g., exceptions and interrupts)*” (see at least paragraph [0028]). Thus, replacing certain system calls with DELI is to mask the events (exceptions and interrupts).

All the amended independent claims have been addressed in connection with the arguments above and therefore have been rejected with detailed explanation above.

Examiner is entitled to give claim limitations their broadest reasonable interpretation in light of the specification. See MPEP 2111 [R-1] Interpretation of Claims-Broadest Reasonable Interpretation. During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification.

Applicant always has the opportunity to amend the claims during the prosecution and broad interpretation by the examiner reduces the possibility that the claims, once issued, will be interpreted more broadly than is justified. In re Prater, 162 USPQ 541, 550-51 (CCPA 1969).

***Allowable Subject Matter***

7. Claims 9-12, 31-34, 44-47, 57, 59 and 60 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Claim Rejections - 35 USC § 101***

8. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 67-68 are rejected under 35 U.S.C. 101 because they are intended to cover signals. The specification provides intrinsic evidence that the computer usable recording medium is intended to cover signals, such are currently not believed to enable the computer usable medium to act as a computer hardware component and realize its functionality absent being claimed in combination with the necessary hardware to receive and convert the signals to computer program logic. Applicant is suggested to amend the claims to recite "removable storage unit".

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

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subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3, 5-7, 13-29, 35-43, 48-55, 61-64 and 66-73 are rejected under 35

U.S.C. 102(e) as being anticipated by Duesterwald et al. (United States Patent Application

Publication No.: US 2003/0101330 A1).

As per claims 1, 27, 53, 67, 69 and 70:

Duesterwald discloses:

- identifying original instructions to be changed while the original instructions are being executed on a processor (see at least paragraph 54 “**intercept the various application instructions that are to be executed**”, also see FIGS. 4-5);
- copying the original instructions to a storage location (see at least paragraph 56 “**fragment is copied to on or more instruction buffer**”, also see FIGS. 4-5);
- adding a jump instruction to the copied instructions to return to a next instruction after the original instruction (see paragraph 54 “**DELI 100 is...injected into the application 102...so as to gain control over its execution**”, also see FIGS. 4-5); and
- replacing the original instructions while the original instructions are in the process of being executed on the processor with mark instructions and a transfer of control to a hook (see at least paragraph 58 “**application instructions are replaced with the patch code that is provided in the associated patch descriptor...**”, also see FIGS. 4-5), see at least paragraph 55 “**DELI 100 jumps back to the application code**”);

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- wherein the original instructions are part of the instruction set of the processor available to a user (see at least paragraph 18 “**code fragment which correspond to the instruction set of the hardware 104**”); and
- wherein a number of times the mark instructions have been executed is countable (see at least paragraph 48 “**code fragments are executed by the application 102 under the control of the DELI 100...DELI 100 can therefore determine which code fragments are used most frequency... can make the determination of which pieces of code are hot**”).

As per claim 2:

Duesterwald discloses:

- prior to the copying step, allowing a write operation on a page in memory wherein the original code is located (**It is inherent in Duesterwald’s approach in order to copy the original instruction into a buffer**).

As per claim 3:

Duesterwald discloses:

- prior to the allocating step, masking interrupts (see at least paragraph 45 “**DELI 100 is injected into the application 102 with the injector 126...gains control over the application and its execution**” – This can consider masking the interrupt of the application).



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As per claim 5:

Duesterwald discloses:

- after the replacing step, unmasking interrupt (see at least paragraph 49 **“DELI 100 jumps back to the application code and the execution of that code is resumed”** – This can consider as unmasking the interrupt of the application after replacing original code with patched code).

As per claims 6, 28 and 54:

Duesterwald discloses:

- wherein the original instructions are changed in reverse order (see at least paragraph 51 **“DELI 100 is to merely optimize the application execution...comprise rearranging and/or reconfiguring the code for better performance”**).

As per claims 7, 29 and 55:

Duesterwald discloses:

- wherein the mark instructions are the same length, in bytes, as the instructions to be changed (see at least paragraph 53 **“...dynamically replace them with new code fragments that do not require that functionality”** – This indicates that the length of patch instruction and the instructions to be changed are the same in order to perform the faulty or missing hardware functionality) .

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As per claims 13, 35 and 61:

Duesterwald discloses:

- enabling functionality of the copied instructions at the storage location (see at least paragraph 49 “**execution of the cached code...**”).

As per claims 14 and 62:

Duesterwald discloses:

- the enabling step comprises reconciling addressing in the instructions in the storage location (see at least paragraph 24 “**the original application’s text segment is still loaded at the same virtual address that it would normally have**”).

As per claim 15:

Duesterwald discloses :

- wherein the enabling step comprises alignment of instructions in the instructions at the storage location (see at least paragraph 51 “**...rearranging and/or reconfiguring the code for better performance**”).

As per claims 16, 36 and 63:

Duesterwald discloses:

- verifying that the original code is susceptible to patching (see at least paragraph 53 “**determine which call upon faulty or missing hardware functionality**”).

As per claims 17, 37 and 64:

Duesterwald discloses:

- wherein the verifying step determines whether any mark instructions are already present in the original instructions (see at least paragraph 53 **“the new code fragments can be cached such that, next time the original code fragments (i.e., a particular function) are required, the new code fragments can be executed with the cached...”** – a **determination must be made in order to know the patched code (marked code) is already exist in the original code**).

As per claim 18:

Duesterwald discloses:

- wherein the verifying step determines whether any copy protect instructions are already present in the original instructions (**Copy protection must be allow in Duesterwald’s approach in order copy the original instructions to storage area**).

As per claim 19:

Duesterwald discloses:

- wherein the verifying step determines whether the original instructions include a suitable jump point that can be modified to the transfer of control to the hook (see at least paragraph 24 **“adding a DELI text segment at the end, and the start symbol (i.e., the entry point that is called by crt0) changed to the DELI entry point”**).

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As per claim 20:

Duesterwald discloses:

- wherein the verifying step determines whether the original instructions represent valid instructions (**the original instructions must be valid instructions in order to perform dynamic patching**).

As per claims 21 and 38:

Duesterwald discloses:

- placing the hook in the memory (see at least paragraph 52 "**several hooks that can be identified to the DELI 100 to permit code fragment replacement**").

As per claim 22:

Duesterwald discloses:

- the hook has been previously placed in memory (see at least paragraph 52 "**several hooks that can be identified to the DELI 100 to permit code fragment replacement**").

As per claims 23, 39 and 66:

Duesterwald discloses:

- wherein the replacing step use an atomic write to replace the original instructions (**It is inherent since there is no changed in instruction length**).

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As per claim 24:

Duesterwald discloses:

- wherein the atomic write replaces one instruction at a time (see at least paragraph 53 **“DELI controls very small portions of code such as code fragments and even individual instructions”**).

As per claim 25:

Duesterwald discloses:

- wherein the atomic write replaces multiple instructions at a time (see at least paragraph 53 **“DELI controls very small portions of code such as code fragments and even individual instructions”**).

As per claim 26:

Duesterwald discloses:

- wherein, for Intel IA-32 architecture, the atomic write uses any of “xchg,” “lock cmpxchg8b,” “lock cmpxchg,” and “lock xchg” instructions (see at least paragraph 57 **“an X86 microprocessor” – any one of the instructions cited can be used in Duesterwald’s approach**).

As per claims 40, 68 ad 71:

Duesterwald discloses:

- identifying original instructions to be changed while the original instructions are being executed on a processor (see at least paragraph 54 **“intercept the various application instructions that are to be executed”**, also see FIGS. 4-5);
- allocating a storage location for storing a functionality equivalent copy of the original instructions (see at least paragraph 21 **“code cache 124”**)
- copying the original instructions to the storage location (see at least paragraph 56 **“fragment is copied to on or more instruction buffer”**, also see FIGS. 4-5); and
- replacing the original instructions while the original instructions are in the process of being executed on the processor with mark instructions and a transfer of control to a hook (see at least paragraph 58 **“application instructions are replaced with the patch code that is provided in the associated patch descriptor...”**, also see FIGS. 4-5), see at least paragraph 55 **“DELI 100 jumps back to the application code”**);
  - o wherein the original instructions are part of the instruction set of the processor available to user (see at least paragraph 18 **“code fragment which correspond to the instruction set of the hardware 104”**); and
  - o wherein a number of times the mark instructions have been executed is countable (see at least paragraph 48 **“code fragments are executed by the application 102 under the control of the DELI 100...DELI 100 can therefore determine which code fragments are used most frequency... can make the determination of which pieces of code are hot”**).

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As per claim 41:

Duesterwald discloses:

- prior to the copying step, allowing a write operation on a page in memory wherein the original code is located (**It is inherent in Duesterwald's approach in order to copy the original instruction into a buffer**).

As per claim 42:

Duesterwald discloses:

- adding a jump instruction to the copied instructions to return to a next instruction after the original instructions (see paragraph 54 "**DELI 100 is...injected into the application 102...so as to gain control over its execution**", also see FIGS. 4-5).

As per claim 43:

Duesterwald discloses:

- wherein the original instructions are changed in reverse order (see at least paragraph 51 "**DELI 100 is to merely optimize the application execution...comprise rearranging and/or reconfiguring the code for better performance**").

As per claim 48:

Duesterwald discloses:

- verifying that the original code is susceptible to patching (see at least paragraph 53 "**determine which call upon faulty or missing hardware functionality**").

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As per claim 49:

Duesterwald discloses:

- wherein the verifying step determines whether any mark instructions are already present in the original instructions (see at least paragraph 53 **“the new code fragments can be cached such that, next time the original code fragments (i.e., a particular function) are required, the new code fragments can be executed with the cached...”** – a determination must be made in order to know the patched code (marked code) is already exist in the original code).

As per claim 50:

Duesterwald discloses:

- wherein the verifying step determines whether any copy protect instructions are already present in the original instructions (**Copy protection must be allow in Duesterwald’s approach in order copy the original instructions to storage area**).

As per claim 51:

Duesterwald discloses:

- wherein the replacing step use an atomic write to replace the original instructions (**It is inherent since there is no changed in instruction length**).

As per claim 52:

Duesterwald discloses:



- enabling functionality of the copied instructions at the storage location (see at least paragraph 49 “**execution of the cached code...**”).

As per claims 72 and 73:

Duesterwald discloses:

- wherein the process of execution of the original instructions is not interrupted throughout the patching process (see at least paragraph 14 “**dynamically patching code, i.e. patching program code while the program is running**”).

### *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 8, 30 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duesterwald et al (United States Patent Application Publication No.: US 20030101330 A1).

As per claims 8, 30 and 56:

Duesterwald does not explicitly disclose:

- wherein the mark instructions are shorter in length, in bytes, as the instructions to be changed, and include NOP (no operation) filler.

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However, Applicant discloses that in the Intel X86 architecture in the specification, when an instruction is changed, its length is never increased (Paragraph 49). It would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize that in Intel X86 architecture, any changed command is either the same length as the original instruction or is shorter with corresponding NOP instructions (no operation) in the remaining bytes.

Therefore, one would have been motivated to use this feature in the Intel X86 architecture for checking to see if the mark instructions are shorter in length, in bytes, as the instructions to be changed or any other useful reason for the invention.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duesterwald et al (United States Patent Application Publication No.: US 20030101330 A1), in view of Scott et al. (United States Patent No.: US 6,615,329).

As per claim 4:

Duesterwald does not explicitly disclose:

- after the replacing step, disallowing (disabling) a write operation on the page in memory where the block of code is located.

However, Scott discloses an analogous method that disable (disallow) a write operation on the page in memory where the block of code is located to protect the area from unauthorized user (**“disable write operations to the protected area”** Col 9,53-54).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Duesterwald's approach to allow disable write operation. One of

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ordinary skill would have been motivated to consider protecting the memory area by disable or disallow a write operation after data have been copied from memory to storage location.

### *Conclusion*

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Duesterwald et al. (United States Patent No.: US 6,915,513 B2) discloses a system and method for dynamically replace code.
- Duesterwald et al. (United States Patent No.: US 6,928,536 B2) discloses a dynamically execution layer interface for replacing instructions requiring unavailable hardware functionality with patch code and caching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571) 270-1070.

The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

P.N.  
11/13/2007

**MARY STEELMAN**  
**PRIMARY EXAMINER**

A handwritten signature in black ink, appearing to read 'Mary Steelman', is written over the printed name and title.